George Mason University

Department of Electrical and Computer Engineering

ECE 680 --- Physical VLSI Design Fall 2008

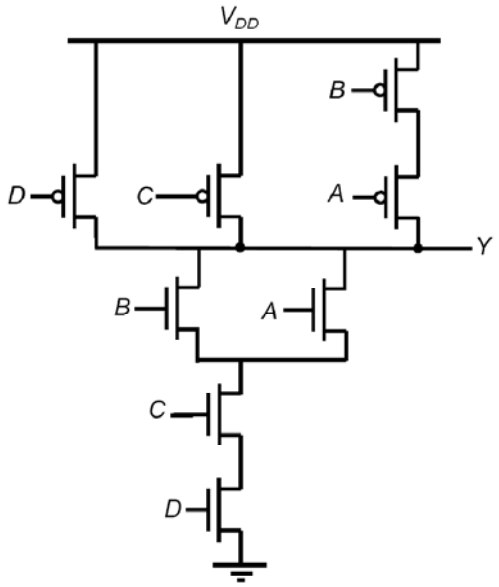
Homework 3 Due: Thursday, 10/16/2008

Policy: Provide details of the solution for each problem. A solution with only final results will not get credit.

Problem 1. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors: (5 inputs, so PUN has 5 transistors and PDN has 5 transistors)

$$\bar{y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

Problem 2. Consider the following CMOS combinational logic circuit




**a.** What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.

**b.** What are the input patterns that give the worst case $t_{pHL}$ and $t_{pLH}$. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

**c.** Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).

**d.** If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume $V_{DD}$=2.5V, $C_{out}$=30fF and $f_{clk}$=250MHz.